April 2003

SEH Silicon Wafers for MEMS and MOEMS Applications

SEH leads the silicon industry as a supplier of bulk and SOI wafers for the MEMS and MOEMS market. The capability and capacity that was developed for the worlds largest manufacturers of inertial and pressure sensors and ink-jet print heads is now available to emerging MEMS and MOEMS companies.

SEH has the broadest product portfolio to supply the needs of any MEMS or MOEMS customer. We manufacture everything from 100mm to 300mm wafers and can supply CZ or FZ material, annealed or fully oxygen precipitated wafers, and a full range of Epi products. Our SOI technology encompasses thick active layer wafers manufactured using our bonding and polishing process, and thin active layer wafers manufactured using the Smart Cut® process. For customers requiring thick active layers with excellent thickness uniformity, our Epi process can be used to produce a hybrid Epi-on-Smart Cut® wafer that offers the best characteristics of both processes.

SEH has the world's largest capacity for production of thick bonded SOI wafers, and we currently supply more than 50% of the SOI wafers used for semiconductor, MEMS, and MOEMS applications.

SEH has a long history of SOI production. Our SOI facility in Nagano was established in 1988, and a new facility was built in 1997 to provide adequate capacity to support the developing micro-technology industry through at least 2010.

SEH can provide unequaled customer support with a team of experienced silicon application engineers located throughout the world.

SEH has wafer-manufacturing facilities in the United States, Japan, Malaysia, Taiwan, and the United Kingdom. Together, these plants supply 28% of global sales, the largest share of the worldwide market for silicon wafers. SEH is owned and supported by Shin-Etsu Chemical, the fifth largest chemical manufacturer worldwide.

PW Wafer Specifications for MEMS Applications

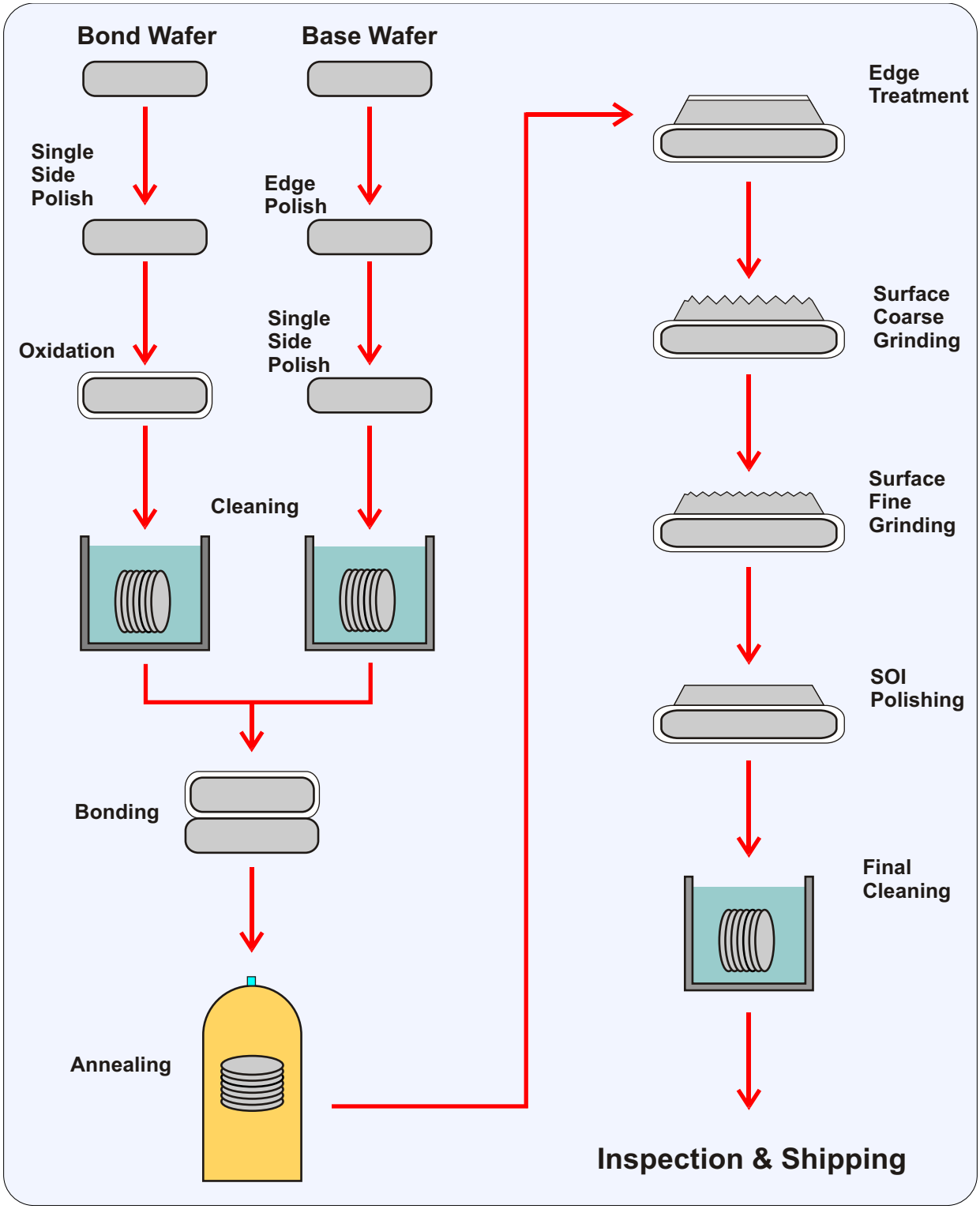
Crystal Specifications						
Growth Method	Czochralski (Float Zone available for special orders)					
Dopant Type	P Type (Boron)		N Type (Phosphorous)		N Type (Antimony)	
Resistivity (ohm.cm)	0.005 – 1	1 – 20	20 – 50	5 – 20	0.013 – 0.02	0.02 – 1
Oxygen (ppma)[1]	20.8 – 28.8	22.4 – 32.0	24.0 – 32.0	24.0 – 32.0	22.4 – 25.6	25.6 – 37.2
Carbon (ppma)[2]	n/a		0.50		n/a	

1. ASTM '79
2. ASTM '75

Specifications by Diameter												
Diameter (mm)	100			125			150			200		
Orientation	<100>, <111>			<100>, <111>			<100>, <111> ,<110>			<100>, <111> ,<110>		
Orientation Tolerance	0.2º			± 0.2º			± 0.2º			± 0.2º		
Thickness (µm)	200 – 650			300 – 700			300 – 750			400 – 725		
Backside Condition	Polish / Etch	Poly	SiO_2 /CVD	Polish / Etch	Poly	SiO_2 /CVD	Polish / Etch	Poly	CVD	Polish / Etch	Poly	SiO_2 /CVD
Bow (µm)	35	n/a	n/a	± 35	n/a	n/a	± 30	± 50	± 30	± 10	n/a	± 15
Warp (µm)	50	n/a	n/a	50	n/a	n/a	30	60	35	35	n/a	50
TTV/GBIR (µm)	4.0			4.0			4.0			6.0		
FPD/GFLD (µm)	0.9			0.9			2.2			n/a		
TIR/GFLR (µm)	1.1			1.1			2.6			4.0		
Edge Finish	22°/Ground			22°/Ground			22°/Ground			22°/Polished		

- SEH can provide both standard and custom designed silicon wafers for any customer's needs. Low Defect Crystal (T3) or Nearly Perfect Crystal (NPC), annealed wafers, Epi wafers, and high-resistivity wafers are all available on request.
- SEH also maintains a large inventory of lower priced stock products for mechanical (machine setup or wafer handling tests), or low COP particle monitor applications.

SOI Process Flow



SOI Specifications for MEMS Applications

Crystal Specifications						
Growth Method	Czochralski or Float Zone					
Crystal Orientation	<100> or <110> ± 1°					
Dopant Type	P Type (Boron)		N Type (Phosphorous)		N Type (Antimony)	
Resistivity (ohm.cm)	0.005 – 1	1 – 20	20 – 50	5 – 20	0.013 – 0.02	0.02 – 1
Oxygen Concentration (ppma)[1]	20.8 – 28.8	22.4 – 32.0	24.0 – 32.0	24.0 – 32.0	22.4 – 25.6	25.6 – 27.2
Carbon Concentration (ppma)[2]	n/a	0.50	0.50		n/a	
Active Layer Thickness						
Active Layer Thickness (µm)	1.5 – 7		7 – 15		15 – 200	
Active Layer Thickness Uniformity (µm)	± 0.5		± 1.0		± 10% (± 3.0 max)	

1. ASTM '79
2. ASTM '75

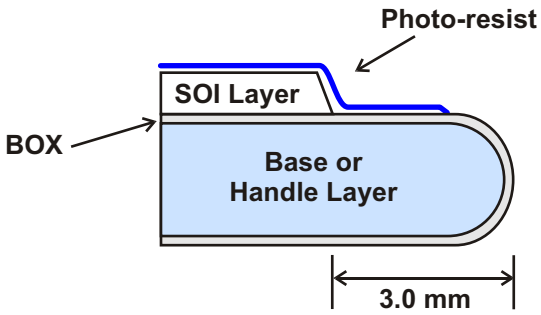
Specifications by Diameter				
Diameter (mm)	100	125	150	200
Handle Layer Thickness (µm)	380 – 425	400 – 625	450 – 675	725
Handle Layer Thickness Uniformity (µm)	25			
Handle Layer Backside Finish	Etched or Polished			
Handle Layer Backside Oxide	Removed by Etching or allowed to remain			
Buried Oxide Layer Thickness				
Buried Oxide Thickness (µm)	0.1 – 0.3		0.5 – 4.0	
Buried Oxide Thickness Uniformity (µm)	15%		5%	

- SOI crystal quality is equivalent to that of a bulk silicon wafer. Low defect, annealed, or high-resistivity crystal is available.
- This specification represents our standard products. SEH has the capability to manufacture wafers with the tightest possible tolerances for customers who need exceptional layer thickness uniformity.
- The lead time for custom designed SOI wafers is very competitive.
- A large inventory of finished SOI products is always available for customers who have an immediate need for research and development material.

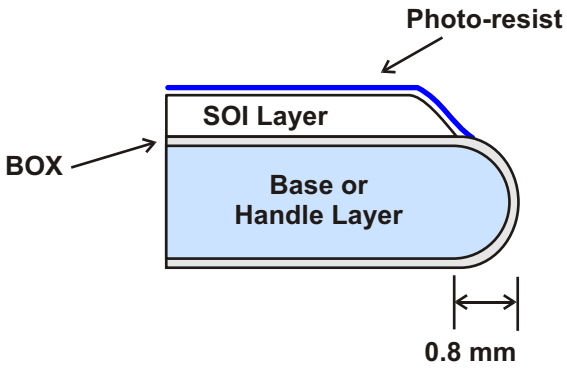
0.8mm Edge Terrace Width (Available for 150mm SOI Wafers)

- Increases the chip yield on a wafer by up to 5% for a 5mm × 5mm device.
- Improves the photo-resist step coverage at the edge of the SOI layer because of the more gentle “roll off” profile.

Industry Standard Edge Terrace



SEH Improved 0.8mm Edge Terrace

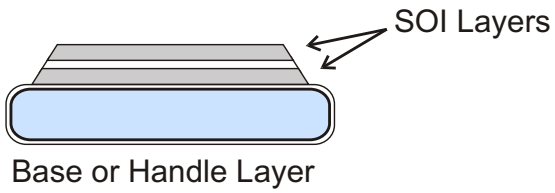


Optional Ion Implanted Buried Layers

An antimony buried layer can be implanted in the active layer at the bonding interface. Doses of 1 × 10^{12} atoms/cm^2 to 3 × 10^{15} atoms/cm^2 are possible at energies of 60 keV to 120 keV

Optional Double Active Layer SOI Wafers

Double Active Layer SOI wafers are available for those who require more complex SOI structures.



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